Remarks

Claims 1-21 remain in this application, with claim 22 being canceled. Clarifying amendments have been made to claims 1, 11, and 19 which simply reorders the wording of the last clause for all 3, and in addition provides antecedent basis. As no change of meaning or scope is intended, we submit no further consideration or search is needed.

Drawings rejection under 37 CFR 1.83(a)

In reply to the Examiner's objection to Fig.4, Applicants have amended this figure to illustrate pointer offsets 522 and 492 when illustrating the change of position of the J1 byte from position 60a (pointer offset 522) to position 54a (pointer offset 492), as described on page 10 lines 8 to 10. Accordingly, the amendment to Fig.4 is not believed to introduce any new matter over that taught in the original description as filed. Withdrawal of the objection under 37 CFR 1.83 (a) is respectfully requested.

Claim rejections under 35 USC 112

With regard to the objection to claim 11 under 35 USC 112 in section 5 of the Official Action, Applicants disagree that the claim is indefinite. However, while not necessary for patentability, have made clarifying amendments to claim 11 which clarify the language without changing claim scope.

Accordingly, we submit claim 11 is clear, and withdrawal of the objection to claim 11 under 35 USC 112 is respectfully requested.

Applicants have amended claim 19 in a similar manner to claim 11.

With regard to the Examiner's objection to claim 21 under 35 USC 112, the subject matter of claim 22 has been included in claim 19 in order to clarify that the provisioning bit is stored in the connection memory, and to provide antecedent basis for the memory in claim 21. In view of its dependency from claim 19, claim 21 is now believed to include the proper antecedent

basis for the term "the memory" which is introduced in claim 19. Withdrawal of the objection to claim 19 under 35 USC 112 is respectfully requested.

Claim Rejections under 35 USC 102

The Examiner maintained his objections to claims 1-6, 11-16, and 19-22 under 35 USC 102 as being anticipated by United Stated Patent No. 5,717,693 (Baydar et al.).

Applicant submit that Baydar does not teach the subject matter as claimed. Without limiting the generality of the foregoing, Baydar does not teach the emphasized portions of claim 1:

> A method for managing latency comprising:
>
> receiving data from high-order synchronous transport module (STM) and synchronous transport signal (STS) sources and low-order tributary unit (TU) and virtual tributary (VT) sources;
>
> providing a provisioning bit for each output; and
>
> synchronizing high-order and low-order outputs by adjusting a pointer for the low-order sources based on the provisioning bit.

The Examiner states in section 8 of the Official Action that the system of Baydar is configured to receive high-order STM signals and STS signals and low-order VT signals and TU signals and adjust a pointer for the low-order sources such that the output of the high order and the low order sources are synchronized.

Applicants respectfully disagree with the Examiner's assessment.

1. Applicants submit that the system of Baydar is not capable of operating in STS mode and VT mode at the same time

Each of independent claims 1, 11, and 19 define receiving data from high-order synchronous transport module (STM) and synchronous transport signal (STS) sources and low-order tributary unit (TU) and virtual tributary (VT) sources, and outputting this data such that high-order and low-order outputs are synchronized.

Applicants submit that the system of Baydar operates in either of the high-order mode **or** low-order mode at a given time. Nowhere does Baydar suggest receiving both types of data at the same time and outputting the two types in a synchronized manner. Applicants refer to the following paragraphs of Baydar to support their position:

"… the receive local interface may provide a STS/STM read address signal **or** a VT/TU read address signal, according to the mode selected." (Col.3 lines 48-50) (Emphasis added)

"The elastic store is designed to be used by an interface in either an STS **or** VT operational mode, multiplexing the RAM addresses and synchronization generated by STS or VT pointer processors, depending upon the operational mode." (Col.3 lines 51-55) (Emphasis added)

"Both multiplexers 2b, 2c are responsive to a mode signal on a line 2n for the purpose of selecting either STS/STM **or** VT/TU mode. This may be provisioned from software." (Col.7 lines 9-12) (Emphasis added)

"The receive section 1 can be provisioned by software to be in STS pointer processing **or** VT pointer processing mode." (Col.6 lines 46-48) (Emphasis added)

After the last paragraph (Col.6 lines 46-48), the description of Baydar splits into two Major parts, a first part that describes the processing of pointers in STS mode starting at column 6 line 48, and a second part that describes the processing of data in VT mode starting at column 14 line 8:

"**In STS pointer processing mode,** the payload received on the line 5 at the line rate is converted to the local network clock rate using the elastic store 3." (Col.6 lines 48-50) (Emphasis added)

"**In the VT pointer processing mode,** the VT pointers are terminated and the elastic store 3 is used to store the V5 synchronization signal and VT payload data for every VT as shown in FIG. 14." (Col.14 lines 8-11) (Emphasis added)

As described in column 6 lines 27-33 with reference to Figs.1a & 1b, the data is inputted in line 5 to "receive section 1" which performs pointer processing in one of the STS **or** VT

modes, and the output is at line 7 (Fig.1b). Mode signal 2n is used to select one operational mode, either STS/STM **or** VT/TU (Col 7 lines 10-12).

The Examiner's attention is respectfully directed to the fact that the main objective of the Baydar reference is to use the same elastic store in either modes, **but not to** process both types at the same time (see Col.4 lines 4-16). Nowhere does Baydar describe processing the two types of data at the same time.

Accordingly, Baydar fails to teach receiving data from high-order synchronous transport module (STM) and synchronous transport signal (STS) sources **and** low-order tributary unit (TU) and virtual tributary (VT) sources, as recited in main claims 1, 11, and 19. (emphasis added)

2. Applicants submit that the system of Baydar does not synchronise low-order outputs and high-order outputs based upon the provisioning bit.

The last clause of claims 1, 11, and 19 have been amended by re-ordering the language of the last clause. For example in claim 1:

~~adjusting a pointer for the low-order sources based on the provisioning bit such that high-order and low-order outputs are synchronized.~~

is changed to:

synchronizing high-order and low-order outputs by adjusting a pointer for the low-order sources based on the provisioning bit.

We point out that this simply reorganizes the clause, without changing the meaning or scope and is therefore not necessary for patentability. However, this rewording emphasizes the difference between the claim and the Baydar reference.

In section 8 of the Official Action, the Examiner states that the high-order and low-order outputs of Baydar are synchronized based upon the mode signal 2n, referring to column 7 lines 8 to 12 of Baydar.

Applicants respectfully disagree with the Examiner, and refer to the circuit shown in Figs.1a &1b (which should be viewed together as stated in column 6 lines 20-21) which illustrate that

the synchronization referred to by the Examiner in section 8 of the Official Action is a synchronization in **writing** the received data into the elastic store (Col.7 lines 6-7) **not in outputting the data therefrom**. The Examiner's attention is respectfully directed to the fact that the output is at line 7, and that Baydar does not include any provisions as to the synchronization of the low-order data and the high-order data at the output by adjusting the pointer for the low-order sources.

Accordingly, Baydar failed to teach inputting data from high-order STS/STM sources **AND** low-order VT/TU sources, as recited in each of main claims 1, 11, and 19, and also failed to teach claims 1, 11, and 19 define synchronizing high-order and low-order outputs by adjusting a pointer for the low-order sources based on the provisioning bit.

Accordingly, the teachings of Baydar fail to teach each and every element of the subject matter claimed in independent claims 1, 11 and 19 and their respective dependent claims. Accordingly, withdrawal of the objection under 35 USC 102(e) is respectfully requested.

Claim Rejections under 35 USC 103

The Examiner has objected to claims 7-10 , 17, and 18 under 35 USC 103 as being obvious in light of the teachings of Baydar. In response, Applicants respectfully request withdrawal of the objections under 35 USC 103 in view of their direct or indirect dependencies from main claims 1, 11, and 19 which are believed to define novel and patentable subject matter.

The Application is now believed to be in a good condition for allowance, and early action in that respect is courteously solicited.

No fee is believed due for this submission. However, Applicant authorizes the Commissioner to debit any required fee from Deposit Account No. 501593, in the name of Borden Ladner Gervais LLP. The Commissioner is further authorized to debit any additional amount required, and to credit any overpayment to the above-noted deposit account.

Respectfully submitted,

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